Q.6 Attempt any two:

i. Design a combinational logic using PLA which produce 3 different outputs which represent following function. **5**

F1= ∑ (1,4,5,12,14,15)
F2= ∑ (3,5,6,8,10,13)
F3= ∑ (0,2,7,11,14,15)

ii. Realize the expression **5**

Y1= AB'C+BC'D'+A'CD',
Y2= BC'D+ABCD+A'C',
Y3= AD'+BC'D+ACD with MUXs, Decoder, Gates and ROM.

iii. What are the different tools for creating a state machine on Chip? Explain all in brief. **5**

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Total No. of Questions: 6 *Total No. of Printed Pages:4*

Enrolment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2017

CS2OE01 Digital Electronics

Programme: Diploma Branch/Specialisation: CS

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. The output of a logic gate is 1 when all its inputs are at logic 0. the gate is either **1**

(a) a NAND or an EX-OR (b) an OR or an EX-NOR
(c) an AND or an EX-OR (d) a NOR or an EX-NOR

ii. DeMorgan's first theorem shows the equivalence of **1**

(a) OR gate and Exclusive OR gate.
(b) NOR gate and Bubbled AND gate.
(c) NOR gate and NAND gate.
(d) NAND gate and NOT gate

iii. In a JK Flip-Flop, toggle means **1**

(a) Set Q = 1 and Q = 0.
(b) Set Q = 0 and Q = 1.
(c) Change the output to the opposite state.
(d) No change in output.

iv. Two bit subtraction is done by **1**

(a) Demultiplexer (b) Multiplexer
(c) Full subtract (d) Half subtract

v. How many flip flops are required to construct a decade counter **1**

(a) 10 (b) 3 (c) 4 (d) 2

vi. ASM chart takes entire block as **1**

(a) 1 unit (b) 2 unit (c) 3 unit (d) 4 unit

vii. Which of the following is the fastest logic **1**

(a) TTL (b) ECL (c) CMOS (d) LSI

viii. Table that is not a part of asynchronous analysis procedure is **1**
(a) Transition table (b) State table
(c) Flow table (d) Excitation table

ix. Which of the memory is volatile memory **1**
(a) ROM (b) RAM (c) PROM (d) EEPROM

x. The access time of ROM using bipolar transistors is about **1**
(a) 1 sec (b) 1 msec (c) 1 microsec (d) 1 nsec.

Q.2 i. Convert The following number in Hexadecimal, Binary and Octal **2**
$(56)_{10}$

ii. Minimize the following expression using K-Map & realize it with NAND Gates. **3**
F=A'B'C'D+A'BC'D+A'B'CD+ABCD'+ABC'D

iii. Design a BCD to Excess-3 Code converter combinational Circuit. **5**

OR iv. Design a combination circuit which can compare two bits long digital number. **5**

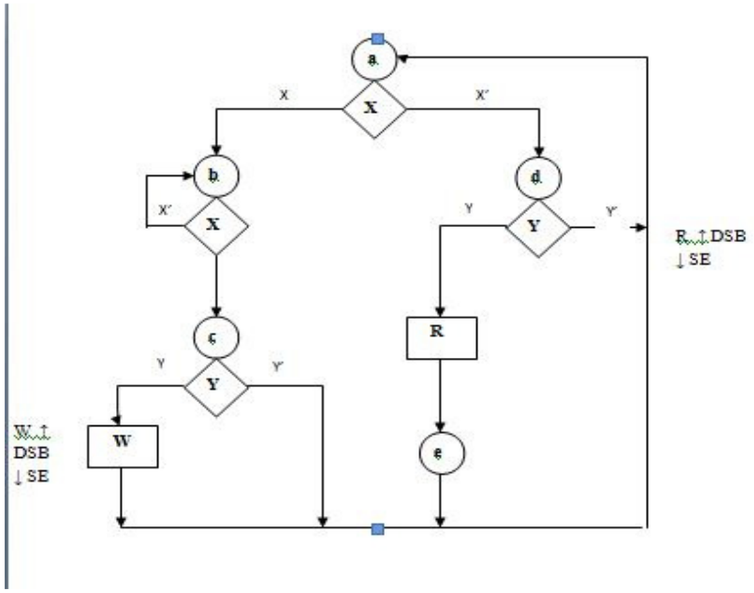
Q.3 i. Explain the working of JK flip-flop. What is the Race-Around Condition? **2**

ii. Design a 4-bit bidirectional shift register and explain its clock diagram in detail. **8**

OR iii. What is Synchronous system? Define the meaning of synchronous state machine. What are the steps of analyzing state machine? **8**

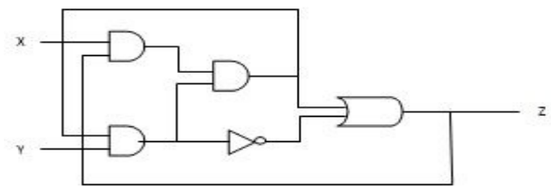
Q.4 i. Design a self starting counter that generate following 3 bit sequence **3**
000, 010, 001, 100, 110, 101, 111, 011

ii. Assuming that data changes on positive clock transition, construct an AST to implement the state diagram of given figure. Use MUX for IFL & Gate for OFL. **7**



OR iii. Construct a reduced state diagram for a system that checks an input line to find the word 110110. The check begins in synchronism with the start of a word and repeat at 6-bit interval. **7**

Q.5 i. For a synchronous circuit given in below figure **4**



Draw the fundamental mode model and label the feedback variables and excitation variable. Also draw the excitation table for circuit.

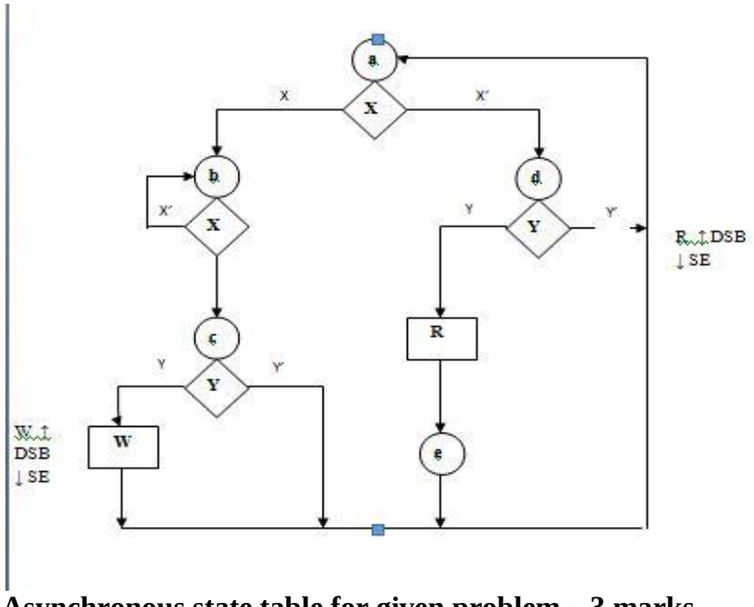
ii. Compare all logic families in tabular form. **6**

OR iii. Explain the interfacing of TTL to CMOS and CMOS to TTL logic. **6**

P.T.O.

CS2OE01 Digital Electronics
Marking Scheme

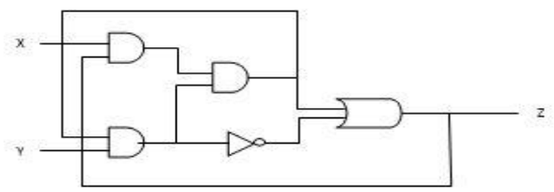
Q.1	i.	The output of a logic gate is 1 when all its inputs are at logic 0. the gate is either (d) a NOR or an EX-NOR	**1**
	ii.	DeMorgan's first theorem shows the equivalence of (b) NOR gate and Bubbled AND gate.	**1**
	iii.	In a JK Flip-Flop, toggle means (c) Change the output to the opposite state.	**1**
	iv.	Two bit subtraction is done by (d) Half subtract	**1**
	v.	How many flip flops are required to construct a decade counter (c) 4	**1**
	vi.	ASM chart takes entire block as (a) 1 unit	**1**
	vii.	Which of the following is the fastest logic (b) ECL	**1**
	viii.	Table that is not a part of asynchronous analysis procedure is (d) Excitation table	**1**
	ix.	Which of the memory is volatile memory (b) RAM	**1**
	x.	The access time of ROM using bipolar transistors is about (c) 1 microsec	**1**
Q.2	i.	Convert The following number in Hexadecimal, Binary and Octal $(56)_{10}$ **Hexadecimal: $(38)_{16}$,** **Binary: $(111000)_2$ and** **Octal: $(70)_8$**	**2**
	ii.	Minimize the following expression using K-Map & realize it with NAND Gates. F=A'B'C'D+A'BC'D+A'B'CD+ABCD'+ABC'D **F = A'B'D + BC'D + ABCD' – 2 marks** **Realization with NAND – 1 mark**	**3**
	iii.	Design a BCD to Excess-3 Code converter combinational Circuit. **BCD to EX-3 Code – 3 marks** **K-map Solution – 1 mark** **Convertor Diagram – 1 mark**	**5**
OR	iv.	Design a combination circuit which can compare two bits long digital number. **Comparator Table – 1 mark** **Comparator Equation – 3 marks** **Circuit Diagram – 1 mark**	**5**
Q.3	i.	Explain the working of JK flip-flop. What is the Race-Around Condition? **JK flip-flop and Race-Around Condition – 2 marks**	**2**
	ii.	Design a 4-bit bidirectional shift register and explain its clock diagram in detail. **Register and its types – 5 marks** **Bidirectional shift register – 3 marks**	**8**
OR	iii.	What is Synchronous system? Define the meaning of synchronous state machine. What are the steps of analyzing state machine? **Synchronous system – 2 marks** **Synchronous state machine – 3 marks** **Steps of analyzing state machine – 3 marks**	**8**
Q.4	i.	Design a self starting counter that generate following 3 bit sequence 000, 010, 001, 100, 110, 101, 111, 011 **Converter table and state diagram – 1 mark** **K-map for input – 1 mark** **Black diagram – 1 mark**	**3**
	ii.	Assuming that data changes on positive clock transition, construct an AST to implement the state diagram of given figure. Use MUX for IFL & Gate for OFL.	**7**



Asynchronous state table for given problem – 3 marks
Use MUX for IFL/OFL – 4 marks

OR iii. Construct a reduced state diagram for a system that checks an input line to find the word 110110. The check begins in synchronism with the start of a word and repeat at 6-bit interval. **7**
State diagram – 3 marks
State table – 2 marks
System diagram – 2 marks

Q.5 i. For a synchronous circuit given in below figure **4**



Draw the fundamental mode model and label the feedback variables and excitation variable. Also draw the excitation table for circuit.
Fundamental mode model – 2 marks
Excitation table for circuit – 2 marks

ii. Compare all logic families in tabular form. **6**
Compare logic families – 3 marks
Table at least five parameters – 3 marks

OR iii. Explain the interfacing of TTL to CMOS and CMOS to TTL logic. **6**
Interfacing – 2 marks
TTL to CMOS – 2 marks
CMOS to TTL – 2 marks

Q.6 Attempt any two:

i. Design a combinational logic using PLA which produce 3 different outputs which represent following function. **5**
F1= ∑ (1,4,5,12,14,15)
F2= ∑ (3,5,6,8,10,13)
F3= ∑ (0,2,7,11,14,15)
PLA with F1, F2 and F3 – 5 marks

ii. Realize the expression **5**
Y1= AB'C+BC'D'+A'CD',
Y2= BC'D+ABCD+A'C',
Y3= AD'+BC'D+ACD with MUXs, Decoder, Gates and ROM.
Realize expression Y1, Y2 and Y3 – 1 mark
MUX – 1 mark
Decoder – 1 mark
Gates – 1 mark
ROM – 1 mark

iii. What are the different tools for creating a state machine on Chip? Explain all in brief. **5**
Tools for creating a state machine – 3 marks
VHDL, Verilog – 2 marks

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